Douglas O. Powell
EN9-99-026 R.A.K

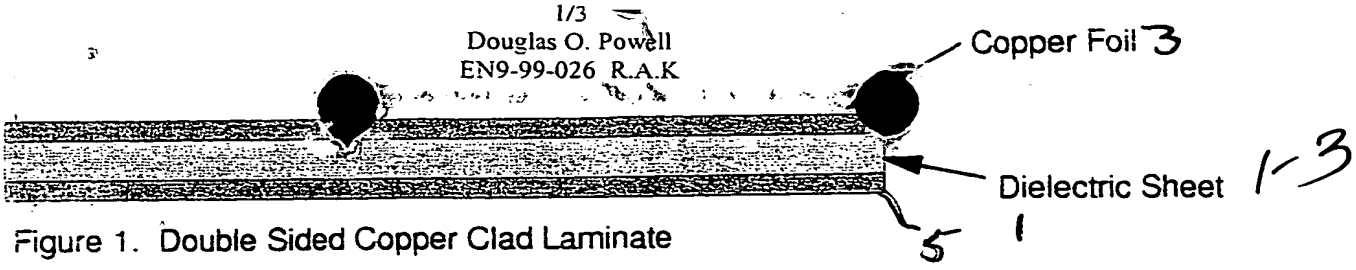

Figure 1. Double Sided Copper Clad Laminate

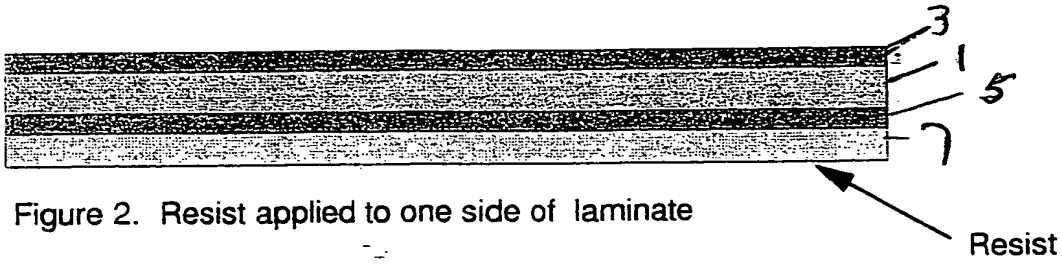

Figure 2. Resist applied to one side of laminate

Figure 3. Copper etched off one side of laminate

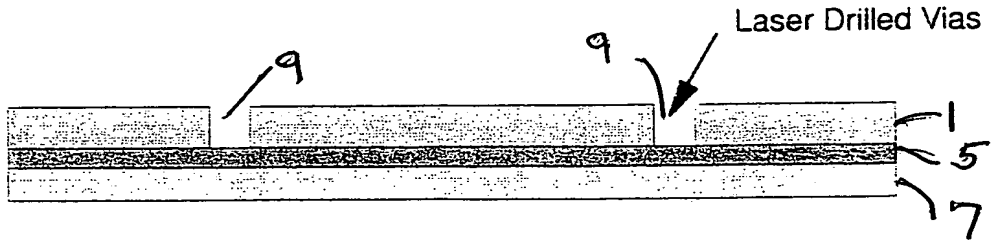

Figure 4. Via holes laser drilled

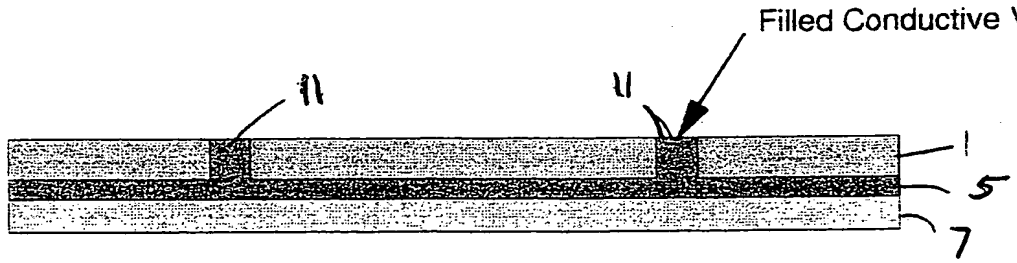

Figure 5. Via holes plated flush

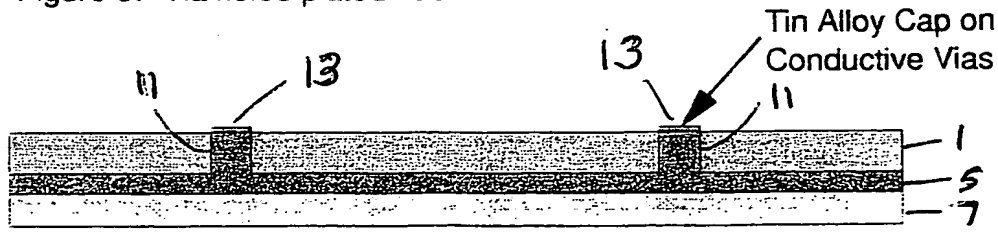

Figure 6. Filled vias overplated with solder alloy

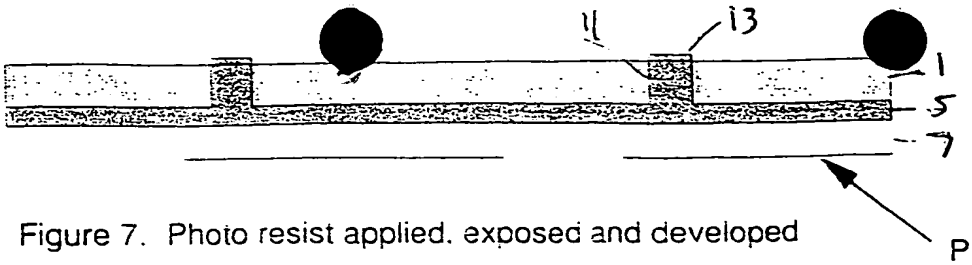

Figure 7. Photo resist applied, exposed and developed

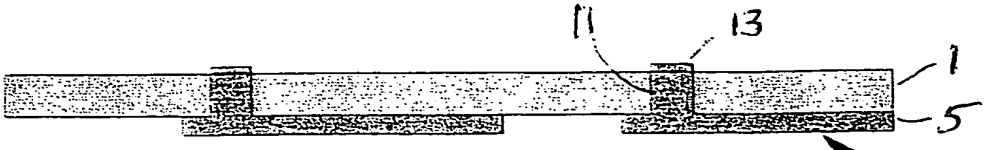

Figure 8. Circuits etched and resist stripped

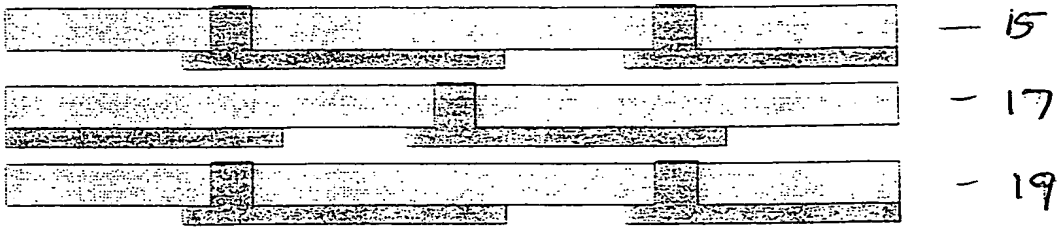

Figure 9. Layers stacked and aligned prior to joining

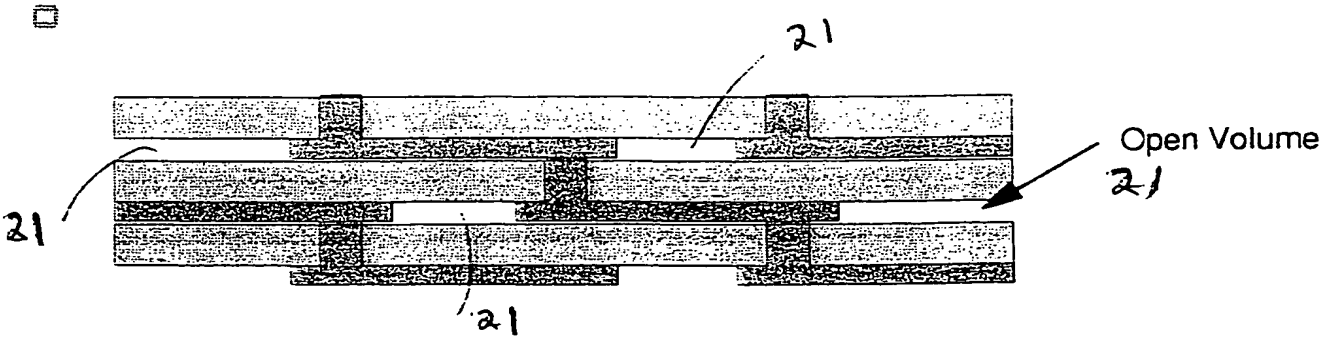

Figure 10. Circuits on adjacent layers joined by soldering

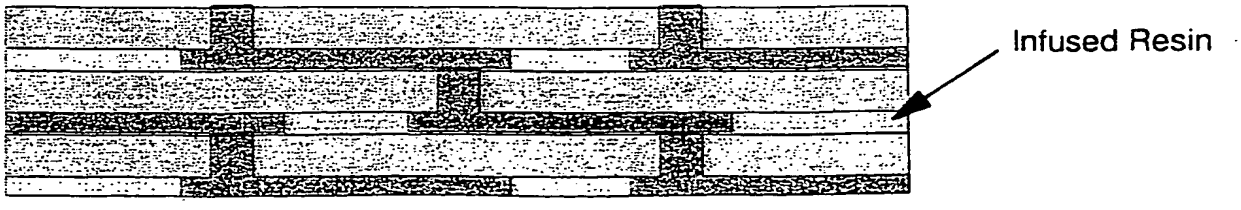

Figure 11. Resin infused and cured to fill and seal open areas

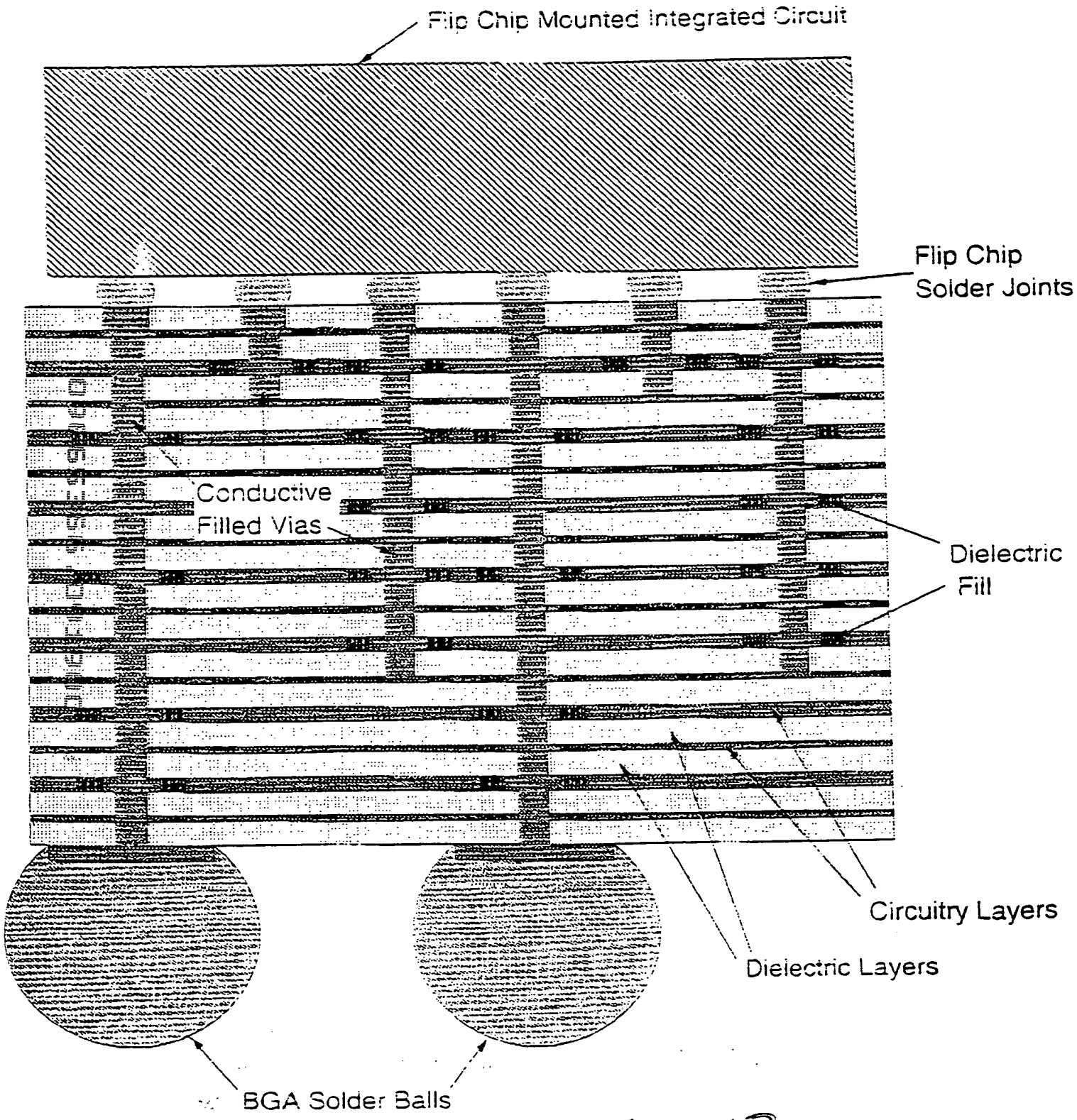
Flip Chip Mounted Integrated Circuit
Flip Chip
Solder Joints
Conductive
Filled Vias
Dielectric
Fill
Circuitry Layers
Dielectric Layers
BGA Solder Balls

Fig. 12